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IN THE CLAIMS

1. (Original) A method of writing a branch instruction into a branch target buffer which comprises a CAM array for holding fetch address data for a plurality of branch instructions and a RAM array for holding target address data for each of said branch instructions, said branch instructions being stored in a computer system at addressable locations having a fetch address and each said branch instruction providing a target address, said method comprising the steps of:

comparing the first selected bits of the fetch address of the branch instruction to be written with first selected bits of the target address of said branch instruction;

in response to a match between said first selected bits of the fetch address and the first selected bits of the target address, writing only second selected bits of the fetch address of said instruction to a CAM location in said CAM array, whereby said second selected bits of the fetch address constitute said fetch address data indicative of the fetch address of said branch instruction; and

writing only second selected bits of the target address to a corresponding RAM location in said RAM array, whereby said second selected bits of the target address constitute said target address data indicative of the target address of said branch instruction, wherein said first selected bits and said second selected bits represent parts of different significance in the fetch address, and wherein said second bits of the fetch address alone provide a test of location in the buffer.

2. (Original) A method according to claim 1 in which a write operation into said branch target buffer is not completed if on comparing said first selected bits of the fetch address and the target address no match is found.

3. (Original) A method according to claim 1 wherein said first selected bits of the fetch address and said first selected bits of the target address represent the bits of higher

significance of said address and said second selected bits of the fetch address and the second selected bits of the target address represent the least significant bits of the address.

4. (Original) A method according to claim 1 in which said branch target buffer comprises a partitioned cache memory and the RAM arrays of the partitions are connected serially in a common data path connected to a cache output, said method further comprising selectively controlling transmission of data along said data path between said RAM arrays so as to designate decreasing priority to partitions connected to the data path on moving away from said cache output and preventing a cache output from any RAM array corresponding to a cache hit which is further from the cache output than the nearest RAM array to the cache output for which a cache hit occurs.

5. (Original) A method of operating a partitioned cache memory as a branch target buffer having a CAM array and a RAM array, the method comprising the steps of:

locating an entry in the branch target buffer using only selected bits of a fetch address stored in the CAM array, wherein the CAM array of each partition is arranged to hold only selected bits of the fetch address of each branch instruction and the RAM array of each partition is arranged to hold only selected bits of the target address of branch instructions in the branch target buffer, and wherein said selected bits of both the fetch address of a branch instruction relate to the least significant bits of the respective address; and

reading the instruction from the buffer in response to the step of locating.

6. (Original) A method according to claim 5 wherein the step of reading the instruction includes providing two input signals relating to fetch address data, a first input comprising some of said selected bits of a fetch address to test for a cache hit in any cache partition responding to said first input, and a second input corresponding to the remainder of said

selected bits of the fetch address, said second input controlling masking circuitry to prevent a cache hit output from any partition not corresponding to data in said second input.

7. (Original) A branch target buffer comprising a partitioned cache memory, each partition comprising a CAM array for holding selected bits of the fetch address of a plurality of branch instructions held in the buffer, a RAM array in each partition coupled to said CAM array and arranged to hold selected bits of a fetch address of branch instructions held in the buffer, said selected bits of the fetch address and selected bits of the said target address each comprising the least significant bits of the respective address, and comparator circuitry for comparing the most significant bits of a fetch address and the most significant bits of the corresponding target address to permit entry of a branch instruction into the buffer only on a match between said most significant bits being found by said comparison circuitry, said least significant bits of said fetch address alone providing test data for locating an entry in the buffer.

8. (Original) A method for accessing a branch target buffer comprising the steps of:

a) comparing first selected bits of a fetch address of a branch instruction to be written with first selected bits of a target address;

b) in response to a match between the first selected fetch address bits and first selected target address bits, writing only second selected bits of the fetch address of said instruction to a CAM location in said CAM array, wherein the second selected bits of the fetch address alone indicate the fetch address of said branch instruction; and

c) writing only second selected bits of the target address to a corresponding RAM location in said RAM array, wherein the second selected bits of the target address indicate the target address of said branch instruction.

9. (Original) The method according to claim 8, wherein step b) is performed only if a match is found between the first selected fetch address bits and first selected target address bits.

10. (Original) The method according to claim 8, wherein the first selected bits of the fetch address and the first selected bits of the target address represent bits of higher significance in the fetch address.

11. (Original) The method according to claim 8, wherein the second selected bits of both the fetch address and the target address indicate a location of a next instruction in the branch target buffer.

Please add the following new claims.

12. (New) A method of writing a branch instruction into a branch target buffer which comprises a first array for holding fetch address data for a plurality of branch instructions and a second array for holding target address data for each of said branch instructions, said branch instructions being stored in a computer system at addressable locations having a fetch address and each said branch instruction providing a target address, said method comprising the steps of:

comparing the first selected bits of the fetch address of the branch instruction to be written with first selected bits of the target address of said branch instruction;

in response to a match between said first selected bits of the fetch address and the first selected bits of the target address, writing only second selected bits of the fetch address of said instruction to a location in said first array, whereby said second selected bits of the fetch address constitute said fetch address data indicative of the fetch address of said branch instruction; and

writing only second selected bits of the target address to a corresponding location in said second array, whereby said second selected bits of the target address constitute said target address data indicative of the target address of said branch instruction, wherein said first selected bits and said second selected bits represent parts of different significance in the fetch address, and wherein said second bits of the fetch address alone provide a test of location in the buffer.

13. (New) A method according to claim 12 in which a write operation into said branch target buffer is not completed if on comparing said first selected bits of the fetch address and the target address no match is found.

14. (New) A method according to claim 12 wherein said first selected bits of the fetch address and said first selected bits of the target address represent the bits of higher significance of said address and said second selected bits of the fetch address and the second selected bits of the target address represent the least significant bits of the address.

15. (New) A method according to claim 12 in which said branch target buffer comprises a partitioned cache memory and the second arrays of the partitions are connected serially in a common data path connected to a cache output, said method further comprising selectively controlling transmission of data along said data path between said second arrays so as to designate decreasing priority to partitions connected to the data path on moving away from said cache output and preventing a cache output from any second array corresponding to a cache hit which is further from the cache output than the nearest second array to the cache output for which a cache hit occurs.

16. (New) A method of operating a partitioned cache memory as a branch target buffer having a first array and a second array, the method comprising the steps of:

locating an entry in the branch target buffer using only selected bits of a fetch address stored in the first array, wherein the first array of each partition is arranged to hold only selected bits of the fetch address of each branch instruction and the second array of each partition is arranged to hold only selected bits of the target address of branch instructions in the branch target buffer, and wherein said selected bits of both the fetch address of a branch instruction relate to the least significant bits of the respective address; and

reading the instruction from the buffer in response to the step of locating.

17. (New) A method according to claim 16 wherein the step of reading the instruction includes providing two input signals relating to fetch address data, a first input comprising some of said selected bits of a fetch address to test for a cache hit in any cache partition responding to said first input, and a second input corresponding to the remainder of said selected bits of the fetch address, said second input controlling masking circuitry to prevent a cache hit output from any partition not corresponding to data in said second input.

18. (New) A branch target buffer comprising a partitioned cache memory, each partition comprising a first array for holding selected bits of the fetch address of a plurality of branch instructions held in the buffer, a second array in each partition coupled to said first array and arranged to hold selected bits of a fetch address of branch instructions held in the buffer, said selected bits of the fetch address and selected bits of the said target address each comprising the least significant bits of the respective address, and comparator circuitry for comparing the most significant bits of a fetch address and the most significant bits of the corresponding target address to permit entry of a branch instruction into the buffer only on a match between said most significant bits being found by said comparison circuitry, said least significant bits of said fetch address alone providing test data for locating an entry in the buffer.

19. (New) A method for accessing a branch target buffer comprising the steps of:

a) comparing first selected bits of a fetch address of a branch instruction to be written with first selected bits of a target address;

b) in response to a match between the first selected fetch address bits and first selected target address bits, writing only second selected bits of the fetch address of said instruction to a location in a first array, wherein the second selected bits of the fetch address alone indicate the fetch address of said branch instruction; and

c) writing only second selected bits of the target address to a corresponding location in a second array, wherein the second selected bits of the target address indicate the target address of said branch instruction.

20. (New) The method according to claim 19, wherein step b) is performed only if a match is found between the first selected fetch address bits and first selected target address bits.

21. (New) The method according to claim 19, wherein the first selected bits of the fetch address and the first selected bits of the target address represent bits of higher significance in the fetch address.

22. (New) The method according to claim 19, wherein the second selected bits of both the fetch address and the target address indicate a location of a next instruction in the branch target buffer.